

**IN THE TITLE**

Please replace the title with the following title:

METHOD AND APPARATUS FOR RESCHEDULING MULTIPLE MICRO-  
OPERATIONS IN A PROCESSOR USING A REPLY QUEUE AND A COUNTER

**IN THE SPECIFICATION**

Please amend the specification as follows:

In one embodiment, allocator/renamer 10 may receive instructions in the form of  $\mu$ ops from front end 4. In one embodiment, each instruction may include the instruction and up to two logical sources and one logical destination. The sources and destination are logical registers (not shown) within processor 2. In one embodiment, a register alias table (RAT) may be used to map logical registers to physical registers for the sources and the destination. Physical sources are the actual internal memory addresses of memory on the chip dedicated to serve as registers. Logical registers are the registers defined by the processor architecture that may be recognized by persons writing assembly language code. For example, according to the Intel Architecture known as IA-32, logical registers include EAX and EBX. Also according to IA-32, such logical registers may be mapped to physical registers, such as, for example, registers 1011 and 1011.